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Patent us6157558 - content addressable memory cell

Content addressable memory cell and array architectures having low transistor counts US 6157558 A

Analysis of power gating in different hierarchical

hierarchical levels of static random-access memory (SRAM) design low-power design in cell of a cell in this memory array is independent of the

Variability aware low leakage reliable sram cell

This paper presents a technique for designing a low power SRAM cell. The cell achieves low power dissipation due to its series connected drivers driven by bitli

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Flash memory - wikipedia, the free encyclopedia

Flash memory stores information in an array of memory cells made from using a floating gate cell design. low-power flash memory that uses a

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